CLAIMS

What is claimed is:

1. A semiconductor device assembly, comprising:

a semiconductor die having a plurality of bond pads on an active surface;

a dielectric film having at least one conductive trace disposed upon a surface thereof and at least one conductive via formed through therethrough;

an electrically conductive layer disposed between the active surface of the semiconductor die and the dielectric film and operably coupled to the at least one conductive via, the electrically conductive layer comprising at least one electrical current isolation slot formed therethrough and a surface providing at least one electrical conductor landing area; and

a plurality of electrical conductors, wherein at least one of the electrical conductors operably couples at least one bond pad to the at least one electrical conductor landing area and at least one other electrical conductor operably couples at least one other bond pad to the at least one conductive trace.

2. The semiconductor device assembly of claim 1, further comprising;

a plurality of discrete conductive elements disposed upon the surface of the dielectric film bearing the at least one conductive trace wherein:

at least one of the discrete conductive elements is operably coupled to the at least one conductive trace; and

at least one additional discrete conductive element is operably coupled to the at least one conductive via.

3. The semiconductor device assembly of Claim 1, wherein the electrically conductive layer includes metal.

4. The semiconductor device assembly of Claim 1, wherein the electrically conductive layer is thermally conductive.

5. The semiconductor device assembly of Claim 1, wherein the electrically conductive layer provides physical support against torsion and bending of the semiconductor device assembly.

6. The semiconductor device assembly of Claim 1, wherein the electrically conductive layer is configured to be operably coupled to a voltage source selected from the group consisting of a ground voltage reference, a power voltage reference, and an intermediate voltage reference.

7. The semiconductor device assembly of Claim 1, wherein the at least one electrical current isolation slot substantially segments the electrically conductive layer into at least two segments wherein high frequency noise present on a voltage source in a first segment of the at least two segments may be substantially isolated from the voltage source in another segment of the at least two segments.

8. The semiconductor device assembly of Claim 1, further comprising;
a longitudinal slot formed through the electrically conductive layer; and
a longitudinal slot formed through the dielectric film having a slot width wider than the longitudinal slot in the electrically conductive layer such that the at least one electrical conductor landing area is exposed through the longitudinal slot in the dielectric film.

9. The semiconductor device assembly of Claim 8, wherein the at least one electrical current isolation slot extends from proximate the longitudinal slot to proximate a lateral peripheral edge of the electrically conductive layer.

10. The semiconductor device assembly of Claim 8, wherein the at least one electrical current isolation slot extends from and is contiguous with the longitudinal slot to proximate a lateral peripheral edge of the electrically conductive layer.

11. The semiconductor device assembly of Claim 8, wherein the at least one electrical current isolation slot intersects and extends from a lateral peripheral edge of the electrically conductive layer to proximate the longitudinal slot.

12. The semiconductor device assembly of Claim 1, wherein the dielectric film further comprises a multi-layer film having at least one additional layer of conductive traces, at least one additional dielectric layer and at least one interlayer conductive via effecting connection between the at least one conductive trace and a conductive trace of the at least one additional layer of conductive traces.

13. The semiconductor device assembly of Claim 1, wherein the electrically conductive layer is adhered to the semiconductor die with a thermally conductive dielectric adhesive layer.

14. The semiconductor package of Claim 13, wherein the thermally conductive dielectric adhesive layer is selected from the group consisting of thermoset adhesives, thermoplastic adhesives, and adhesive tape.

15. The semiconductor device assembly of Claim 1, further comprising a dielectric encapsulant forming a protective structure over the plurality of bond pads and the plurality of electrical conductors.

16. A package substrate, comprising:

a dielectric film having at least one conductive trace disposed upon a top surface thereof and at least one conductive via formed therethrough; and

an electrically conductive layer adhered to the dielectric film and operably coupled to the at least one conductive via, the electrically conductive layer comprising at least one electrical current isolation slot formed therethrough and a surface providing at least one electrical conductor landing area.

17. The package substrate of Claim 16, further comprising;

a plurality of discrete conductive elements disposed upon the surface of the dielectric film bearing the at least one conductive trace wherein;

at least one of the plurality of discrete conductive elements is operably coupled to the at least one conductive trace; and

at least one additional discrete conductive element of the plurality is operably coupled to the at least one conductive via.

18. The package substrate of Claim 16, wherein the electrically conductive layer includes metal.

19. The package substrate of Claim 16, wherein the electrically conductive layer is thermally conductive.

20. The package substrate of Claim 16, wherein the electrically conductive layer provides physical support against torsion and bending of the package substrate.

21. The package substrate of Claim 16, wherein the electrically conductive layer is configured to be operably coupled to a voltage source selected from the group consisting of a ground voltage reference, a power voltage reference, and an intermediate voltage reference.

22. The package substrate of Claim 16, wherein the at least one electrical current isolation slot substantially segments the electrically conductive layer into at least two segments wherein high frequency noise present on a voltage source in a first segment of the at least two segments may be substantially isolated from the voltage source in another segment of the at least two segments.

23. The package substrate of Claim 16, comprising;
a longitudinal slot formed through the electrically conductive layer; and
a longitudinal slot formed through the dielectric film having a slot width wider than the longitudinal slot in the electrically conductive layer such that the at least one electrical conductor landing area is exposed through the longitudinal slot in the dielectric film.

24. The package substrate of Claim 23, wherein the at least one electrical current isolation slot extends from proximate the longitudinal slot to proximate a lateral peripheral edge of the electrically conductive layer.

25. The package substrate of Claim 23, wherein the at least one electrical current isolation slot extends from and is contiguous with the longitudinal slot to proximate a lateral peripheral edge of the electrically conductive layer.

26. The package substrate of Claim 23, wherein the at least one electrical current isolation slot intersects and extends from a lateral peripheral edge of the electrically conductive layer to proximate the longitudinal slot.

27. The package substrate of Claim 16, wherein the dielectric film further comprises a mutli-layer film having at least one additional layer of conductive traces, at least one additional dielectric layer and at least one interlayer conductive via effecting connection between the at least one conductive trace and a conductive trace of the at least one additional layer of conductive traces.

28. A method of making a semiconductor device assembly comprising:

forming at least one electrical current isolation slot in an electrically conductive layer; and

adhering the electrically conductive layer to a dielectric film bearing at least one conductive trace and at least one conductive via therethrough such that the at least one conductive via operably couples to the electrically conductive layer.

29. The method of claim 28, further comprising;

locating a plurality of discrete conductive elements on a surface of the dielectric film such that at least one of the discrete conductive elements operably couples to the at least one conductive trace and at least one other discrete conductive element operably couples to the at least one conductive via.

30. The method of Claim 28, further comprising:

attaching a semiconductor die having a plurality of bond pads on an active surface thereof to a surface of the electrically conductive layer with a thermally conductive dielectric adhesive layer.

31. The method of Claim 30, further comprising:

providing a plurality of electrical conductors to the semiconductor die to operably couple at least one of the plurality of electrical conductors between at least one of the plurality of bond pads and the electrically conductive layer and at least one other electrical conductor between at least one other bond pad and the at least one conductive trace.

32. The method of Claim 31, further comprising;

forming a longitudinal slot through the electrically conductive layer; and

forming a longitudinal slot through the dielectric film; and wherein the plurality of electrical conductors are operably coupled through the longitudinal slot through the conductive layer and the longitudinal slot through the dielectric film.

33. The method of Claim 31, further comprising dielectrically encapsulating the plurality of electrical conductors and the plurality of bond pads.

34. The method of Claim 28, further comprising:

singulating the semiconductor device assembly from a strip comprising a plurality semiconductor device assemblies.

35. The method of Claim 34, wherein singulating the semiconductor device assembly is selected from the group consisting of sawing, punching, and laser ablation.

36. The method of Claim 28, wherein adhering the electrically conductive layer is achieved using a thermally conductive dielectric adhesive.